IN THE CLAIMS:

Claims 1-13 (Canceled).

Claim 14 (Original): A method of fabricating a semiconductor package for three-dimensional mounting, comprising:

(a) placing a semiconductor chip on an upper surface of a substrate, said substrate having the upper surface on which a first metal pattern is formed and a lower surface on which a second metal pattern is formed, said first metal pattern and second metal pattern being electrically connected to each other;

(b) electrically connecting the semiconductor chip and the first metal pattern to each other;

(c) sealing the semiconductor chip and the first metal pattern with sealing resin; and

(d) forming, in the sealing resin, a through hole which reaches the first metal pattern, and forming a wire inside the through hole to electrically connect to the first metal pattern.

Claim 15 (Original): A method according to claim 14, wherein the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin.

Claim 16 (Original): A method of fabricating a semiconductor package for three-dimensional mounting, comprising:

(a) preparing a substrate;

(b) forming a first metal pattern on an upper surface of the substrate;

(c) forming a second metal pattern on a lower surface of the substrate;

(d) electrically connecting the first metal pattern and the second metal pattern to each other;

(e) placing a semiconductor chip on the upper surface of the substrate;

(f) electrically connecting the semiconductor chip and the first metal pattern to each other;

(g) sealing the semiconductor chip and the first metal pattern with sealing resin;

(h) forming a through hole extending from the surface of the sealing resin to the first metal pattern; and

(i) forming a wire inside the through hole.

Claim 17 (Original): A method according to claim 16, wherein the through hole is formed by irradiating a laser beam onto a predetermined position of the surface of the sealing resin.

Claim 18 (Original): A method according to claim 14, further comprising:

(a) disposing a second substrate on the sealing resin after forming the wire inside the through hole; and

(b) electrically connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other.

Claim 19 (Original): A method according to claim 14, wherein said placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising:

separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole.

Claim 20 (Original): A method according to claim 14, further comprising:

(a) forming a fourth wire on the surface of the sealing resin after forming the wire inside the through hole, the fourth wire being electrically connected to one end of the wire;

(b) forming an insulating layer on the fourth wire; and

(c) forming a third electrode which is electrically connected to the fourth wire and exposed from the insulating layer.

Claim 21 (Original): A method according to claim 16, further comprising:

(a) disposing a second substrate on the sealing resin after forming the wire inside the through hole; and

(b) electrically connecting the wire formed inside the through hole and a third metal pattern formed on the second substrate to each other.

Claim 22 (Original): A method according to claim 16, wherein said placing a semiconductor chip includes placing a plurality of semiconductor chips on the upper surface of the substrate, the method further comprising:

separating the plurality of semiconductor chips from each other to obtain a plurality of semiconductor packages after forming the wire inside the through hole.

Claim 23 (Original): A method according to claim 16, further comprising:

(a) forming a fourth wire on the surface of the sealing resin after forming the wire inside the through hole, the fourth wire being electrically connected to one end of the wire;

(b) forming an insulating layer on the fourth wire; and

(c) forming a third electrode which is electrically connected to the fourth wire and exposed from the insulating layer.